



CPSSC 2021

PCB Based Integrated Magnetics

- *Benefits and Limitations* -

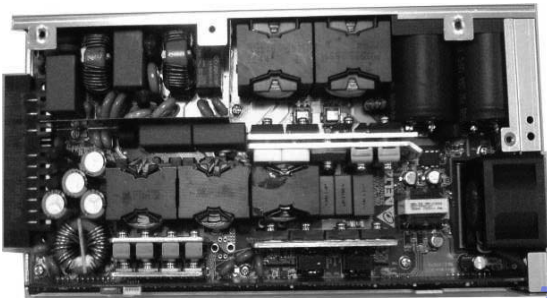
Fred C Lee

CPES
Virginia Tech

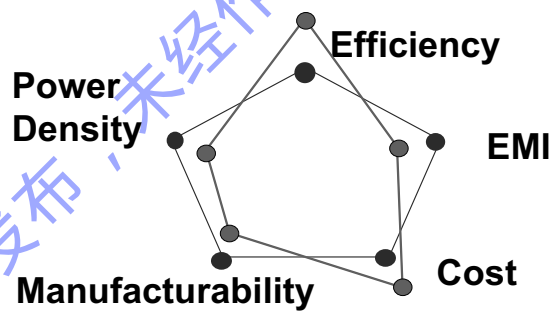
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State-of-the-Art Server Power Supplies

SOA silicon based design
has reach a point of maturity in performance optimization



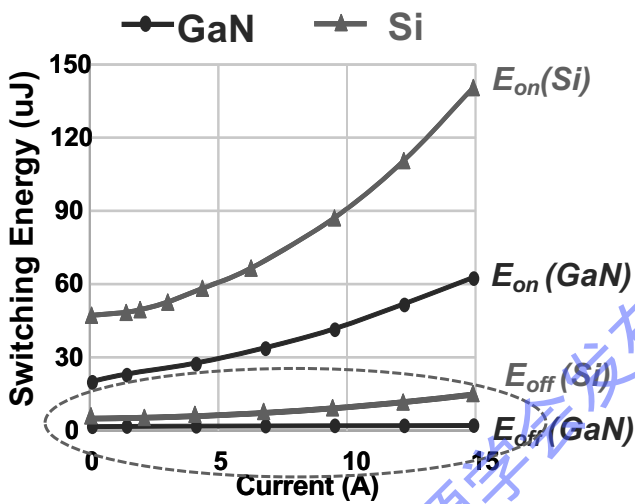
1KW Server power supplies



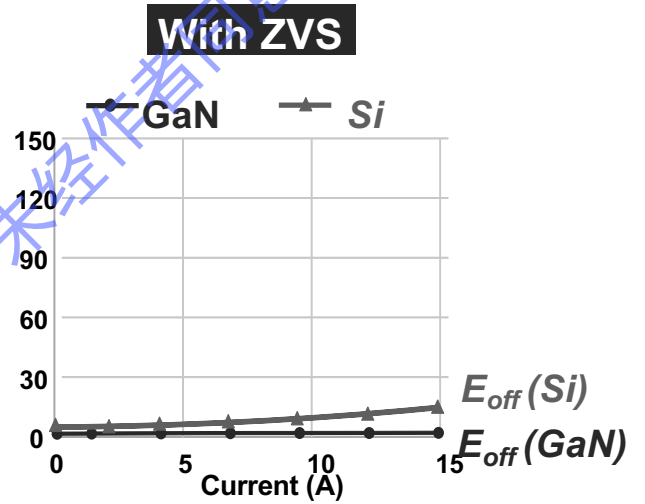
Trade offs:
efficiency, power density and Cost

Unsolved Issues: **EMI & Manufacturability**

GaN vs Silicon MOSFET



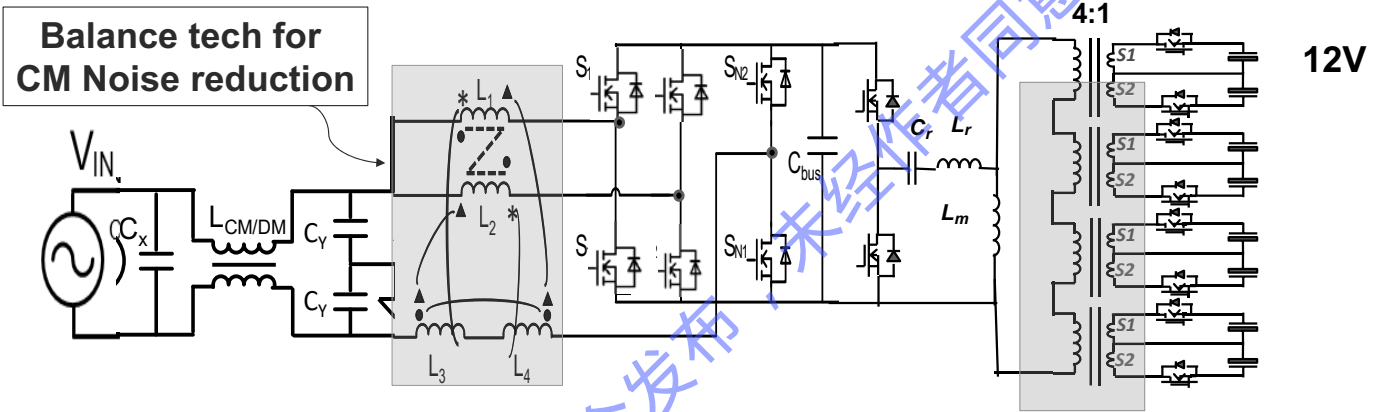
GaN: 3X better



GaN: 10 - 20X better

What would you do if there is no switching related loss??

GaN-Based 1kW Server Power Supplies



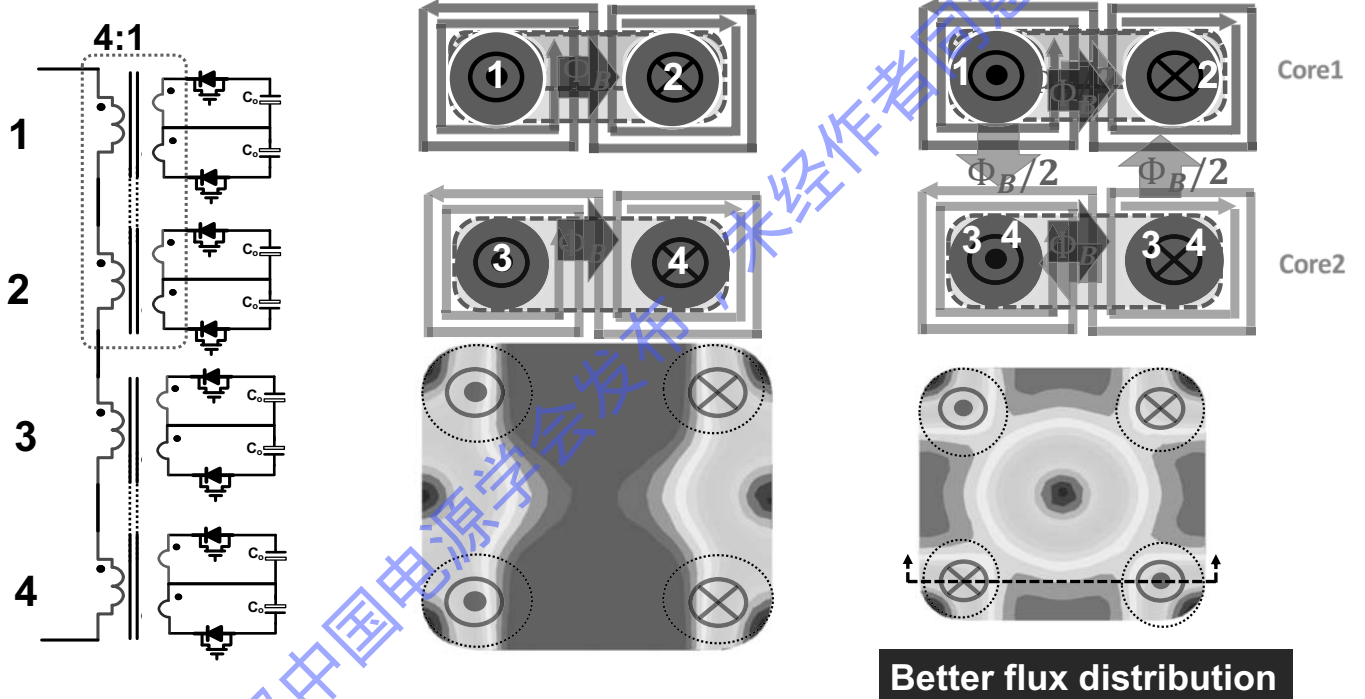
Totem-pole PFC

- > 1MHz
- CRM with ZVS
- PCB Based integrated inductors

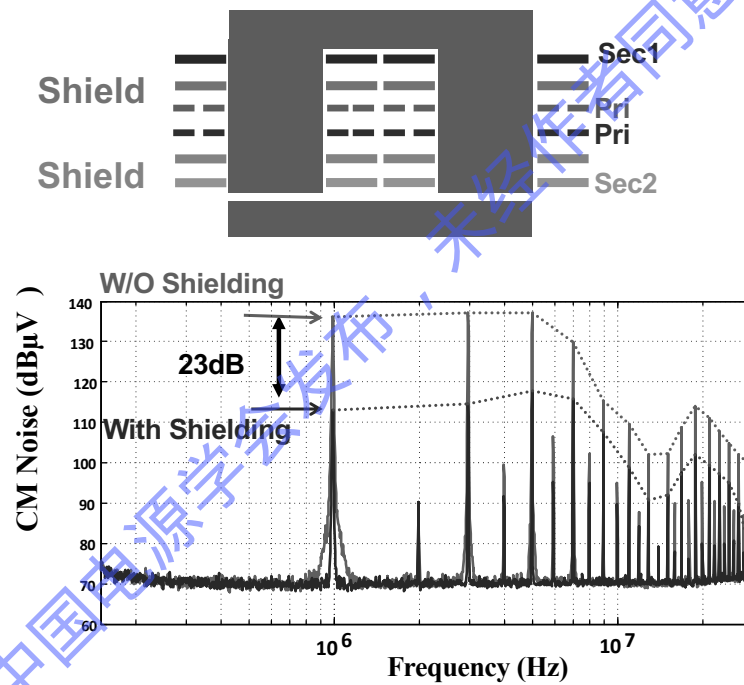
LLC D2D

- > 1MHz
- PCB based integrated L&T

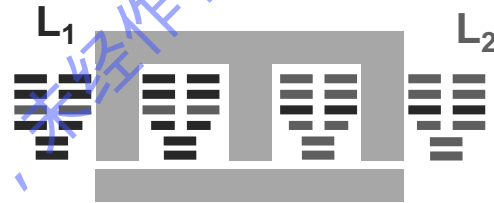
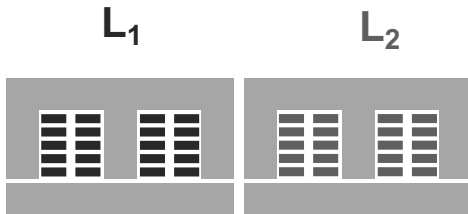
Feature 1: Integrated Transformers in PCB





Feature 2: CM Noise Reduction by Shielding



Feature 3: Integrated Inductors in PCB

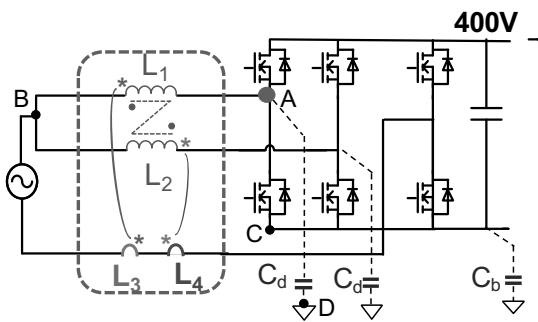


| | Winding (W) | Core Loss (W) | Total Loss (W) |
|---|-------------|---------------|----------------|
| PCB Winding | 6.7 | 1.3 | 8.0 |
|  | 2.3 | 2.3 | 4.6 |

| | Winding(W) | Core Loss (W) | Total Loss (W) |
|---|------------|---------------|----------------|
| 6-Layer with Winding Cut | 2.4 | 1.9 | 4.3 |
|  | 2.3 | 2.3 | 4.6 |

Total loss is smaller than Litz wire inductor

Feature 4: Reducing CM Noise by Balance



PCB embedded coupled inductor

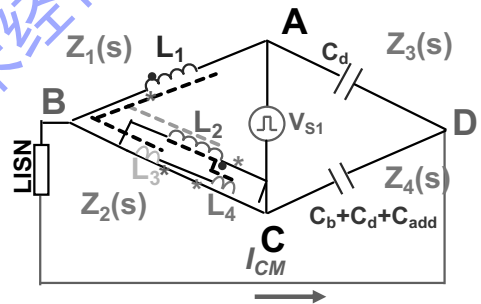


L₃ & L₄ are free gifts

*CM Noise Equivalent Circuit

Apply superposition to V_{S1}

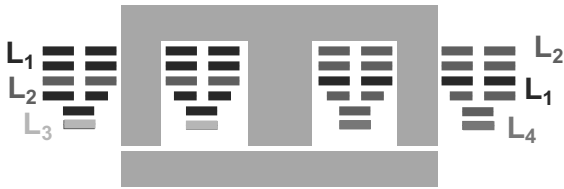
Wheatstone Bridge



Balance Condition

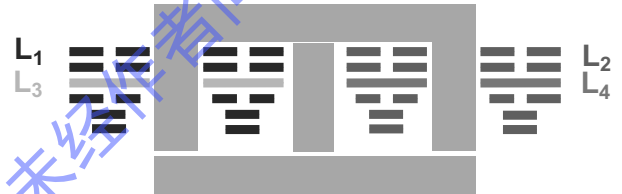
$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4} \quad I_{CM} = 0$$

Further Reduction of CM Noises in High Frequency

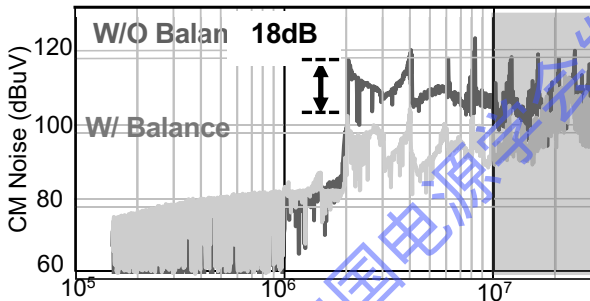


$$\alpha_{12} = -0.6; \quad \alpha_{13} = 0.96$$

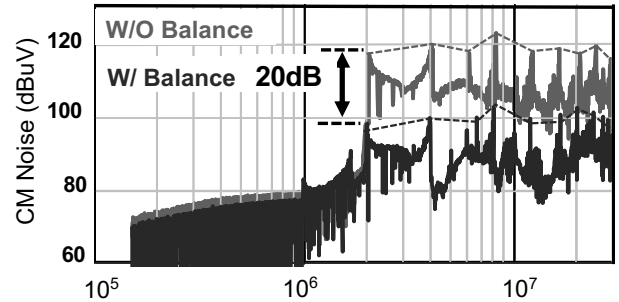
Improved Structure



$$\alpha_{12} = -0.6; \quad \alpha_{13} \approx 1$$

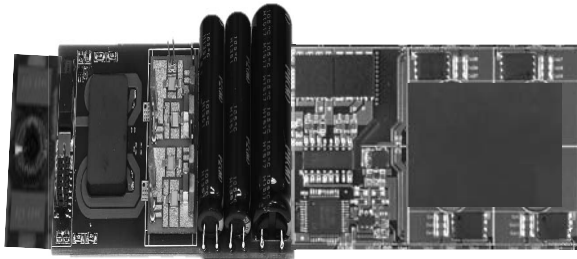


20dB CM noise reduction under 10 MHz

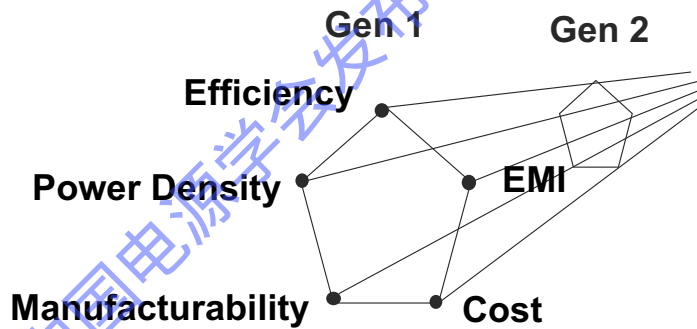


20dB CM noise reduction up to 30 MHz

Is GaN A Game Changer ?

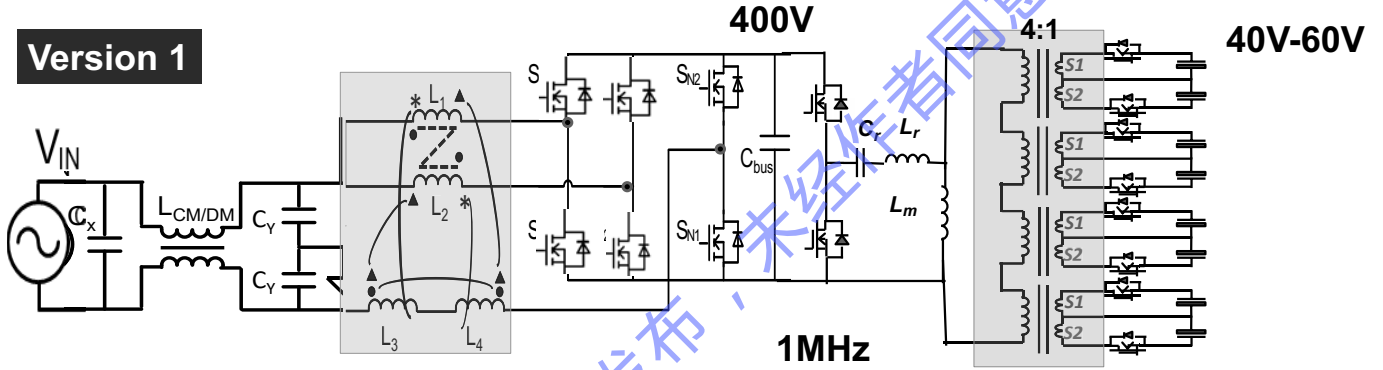


Eff \approx 98%
Power density $>$ 5X
Improved EMI \approx 20dB
Automated Manufacturing
Low Cost



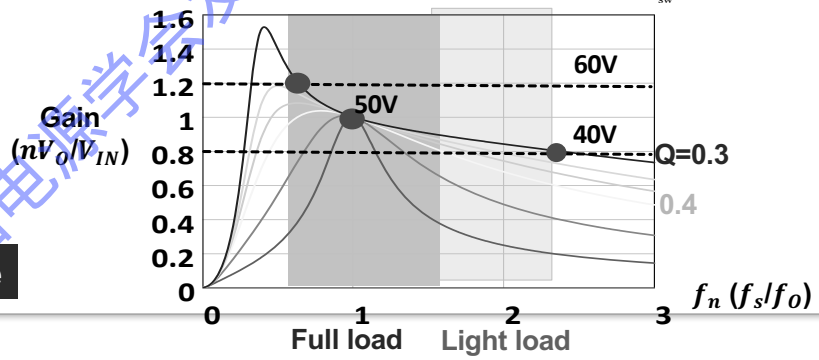
**Can we repeat the success of
PCB based Integrated Inductors and Transformers
at Higher Power Level ?**

3kW Server Power Supplies

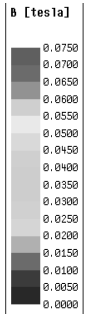
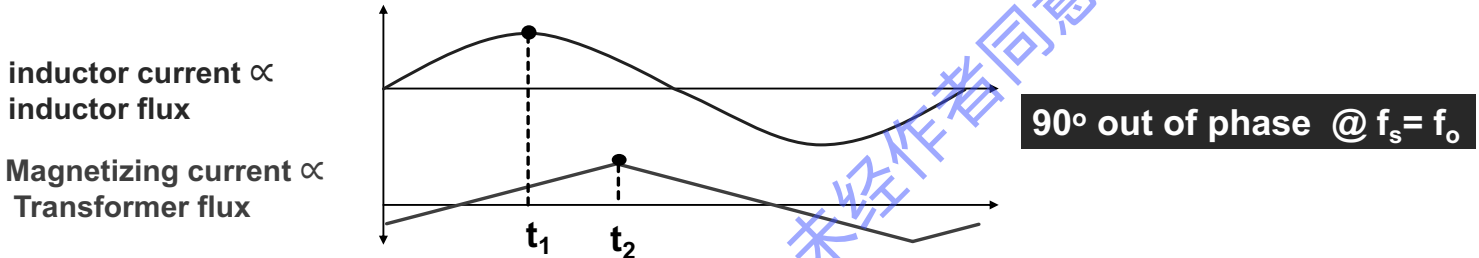


Need gain control

Wide frequency range



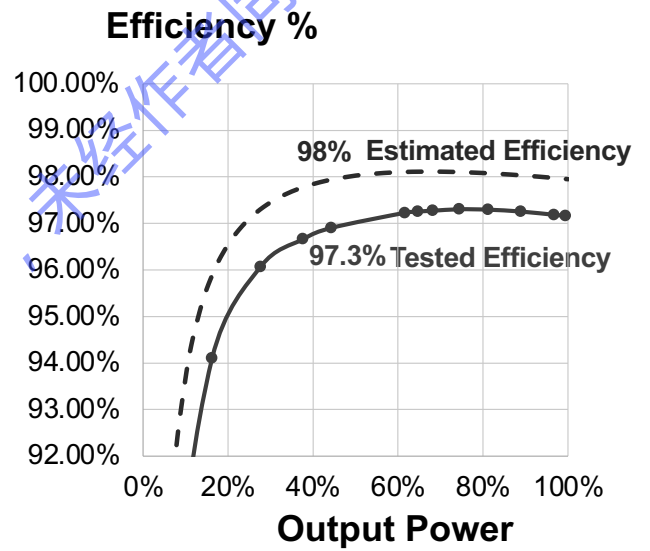
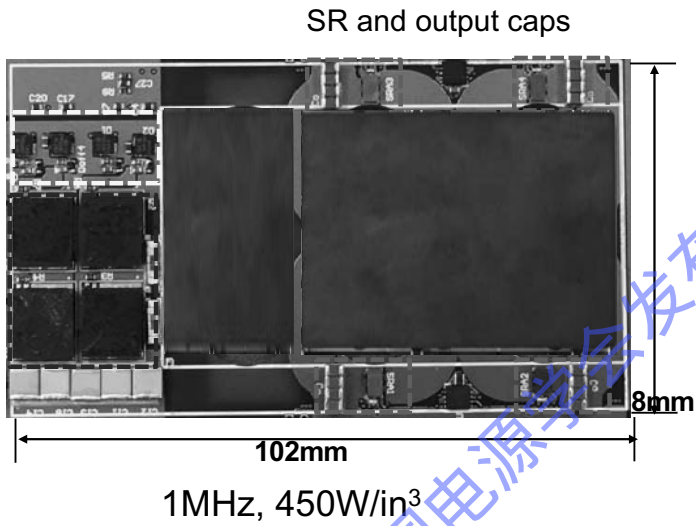
Integration of Inductor and Transformers



30% Less core loss in plates

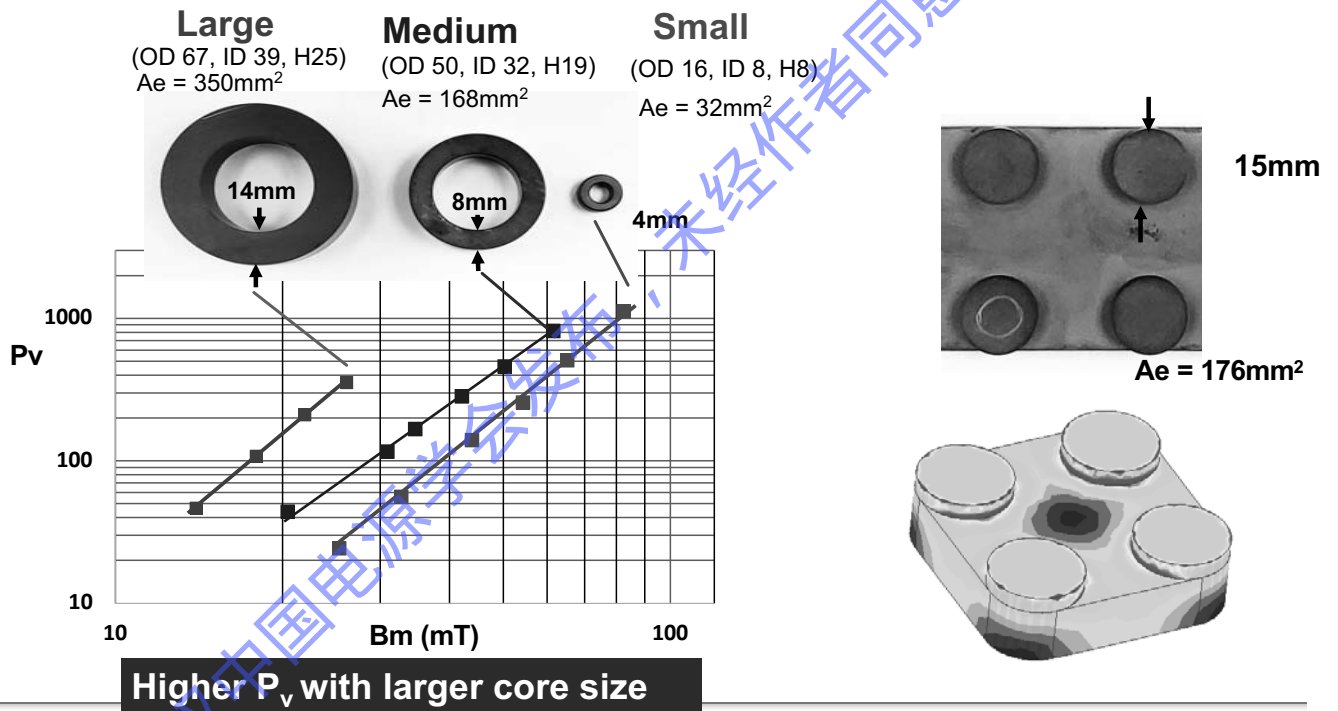
Version 1: Hardware Prototype

Fs=1MHz, Lm=16uH, Lr=4uH, Cr=6.2nF, td=65ns



Significant difference between tested and estimated efficiency

Impact of Core Size on Core Loss

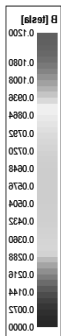


Issues: Eddy Loss and Skin Effect in large Cores

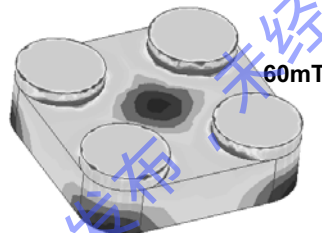
Case 1:
1KW @ 12V & 1MHz

Case 2:
3KW @ 48V & 1MHz

Eddy Loss density:



4X
→



$$P_{eddy} = \frac{1}{4} \sigma \pi (B_m^2 f^2 A_e)$$

0.7W Loss
(20% Eddy Loss)

10W Loss
(60% Eddy Loss)

σ = material conductivity

B_m = max flux density

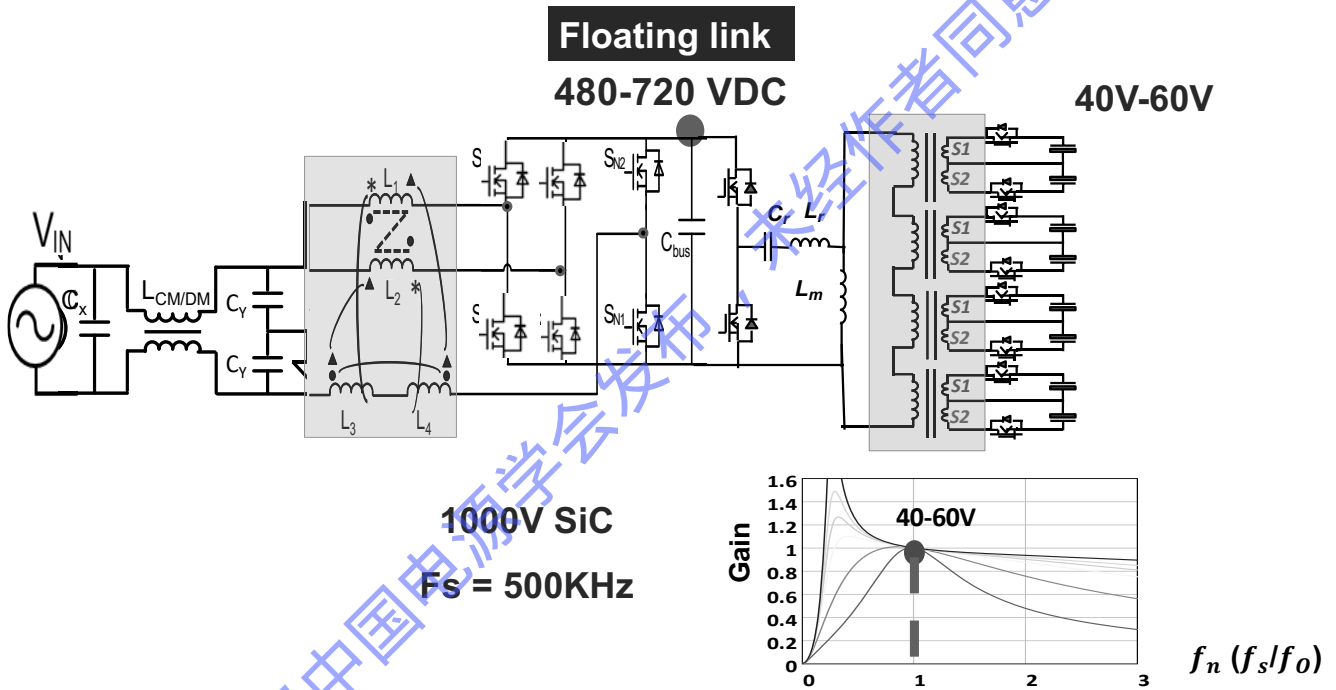
f = frequency

A_e = cross section Area

Core loss density increases disproportionately

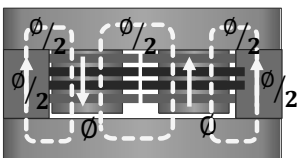
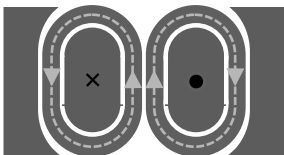
About 70-80% core loss is on the plates

Improvement 1 : DCX with Floating Bus Voltage

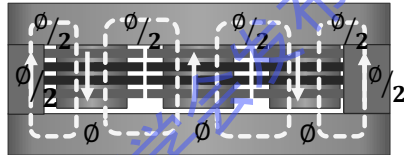
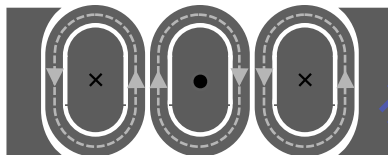


Improvement 2: Planer Magnetic Design

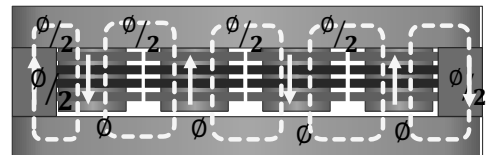
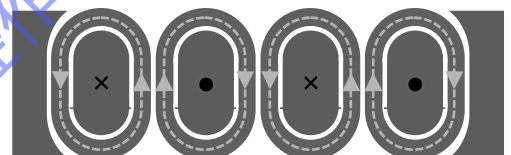
2-Transformers



3-Transformers ✓

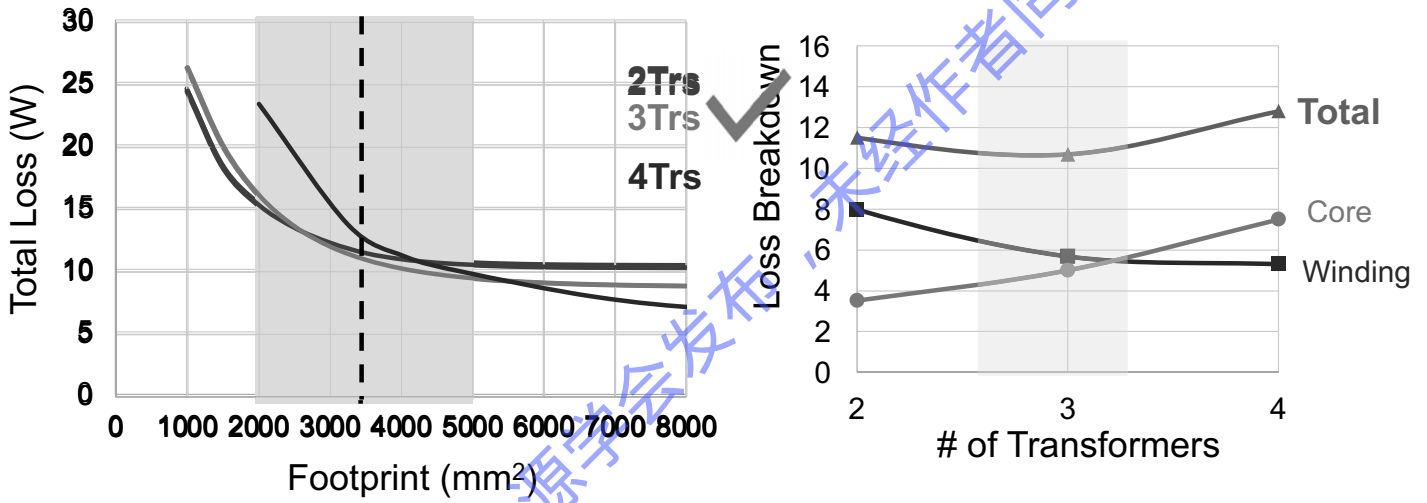


4-Transformers



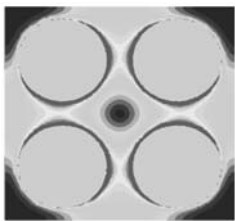
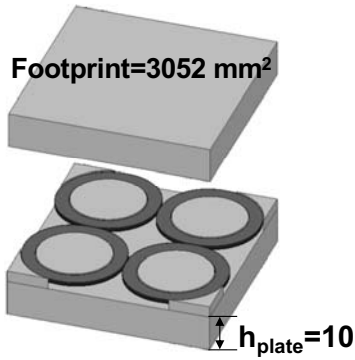
B_m in the plates = $0.5B_m$ in the posts; thus with reduced eddy loss

Optimum Number of Transformers



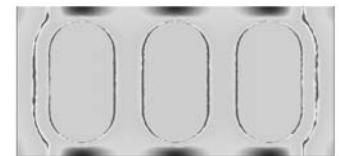
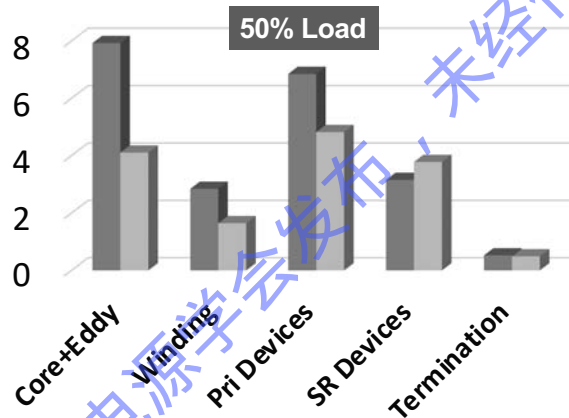
❖ 1-Transformer per kW is deemed optimal

Improvement 2: Transformer Design



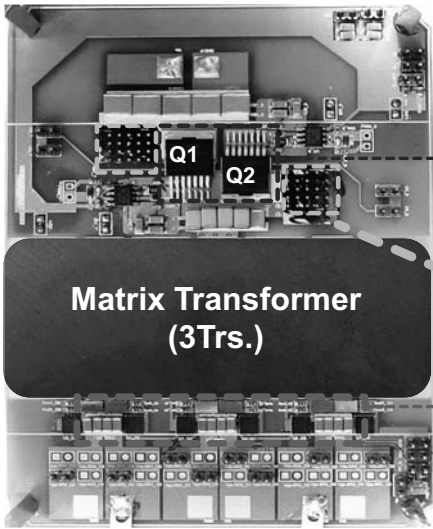
4x 900V SiC MOSFET
16x 80V GaN SR

■ 4Trs (500kHz) ■ 3Trs (HB - 500kHz)



2x 900V SiC MOSFET
12x 80V GaN SR

Hardware Prototype

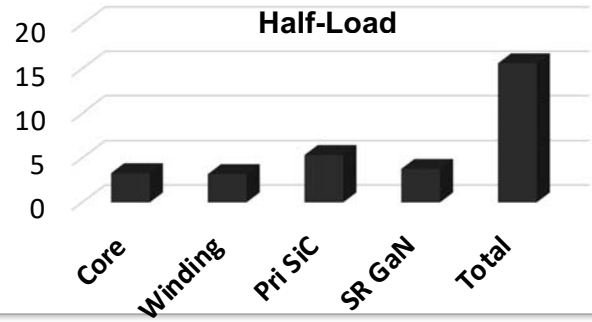
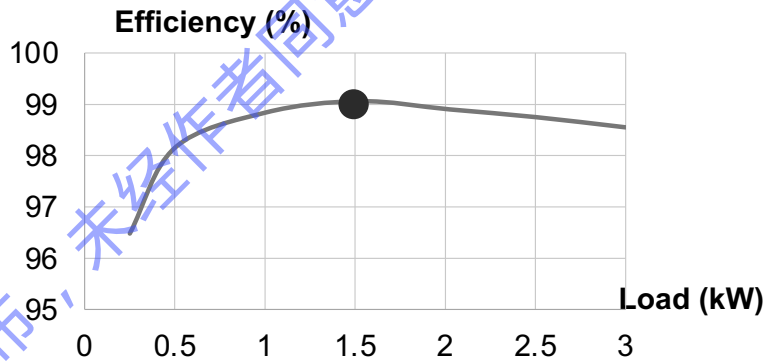


Half-Bridge
(900V SiC)

Thermal Vias
(To cool the SiC)

3-Rectifiers
(80V GaN)

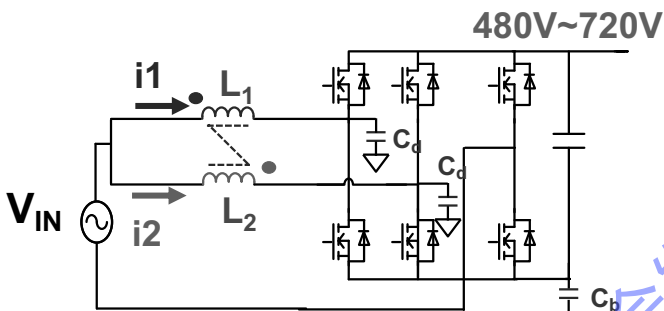
$L_m=32 \mu\text{H}$ $L_k = 0.260 \mu\text{H}$ $C_r = 420 \text{ nF}$
 $F_s = 470 \text{ kHz}$ $T_d=85 \text{ ns}$ Load = 3 kW (100%)



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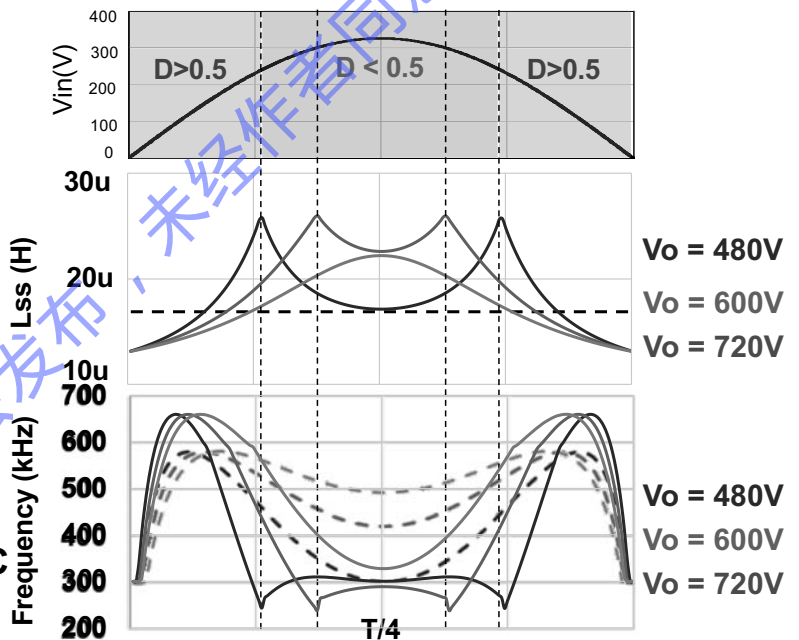
PFC with Variable Link Voltage

Negative coupling
 $\alpha = -0.6$



L1 & L2 are positively coupled

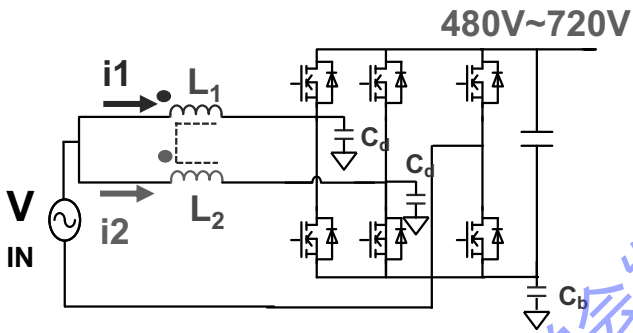
Design is different from 1KW PFC



Negative coupled inductor has larger f_{sw} range than non-coupled inductor

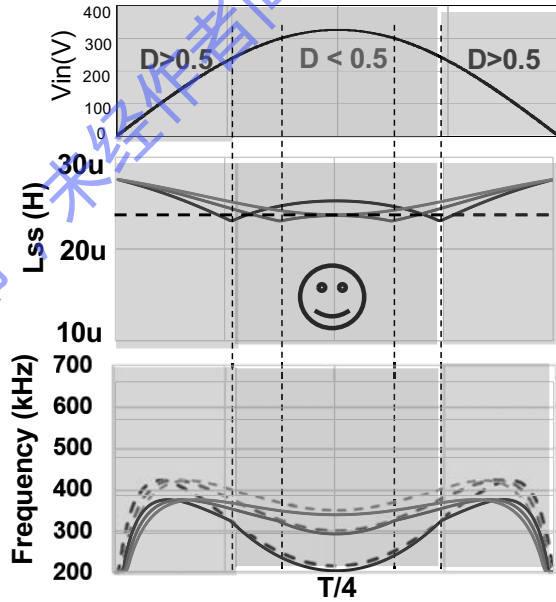
PFC with Variable Link Voltage

Positive coupling
 $\alpha = 0.2$



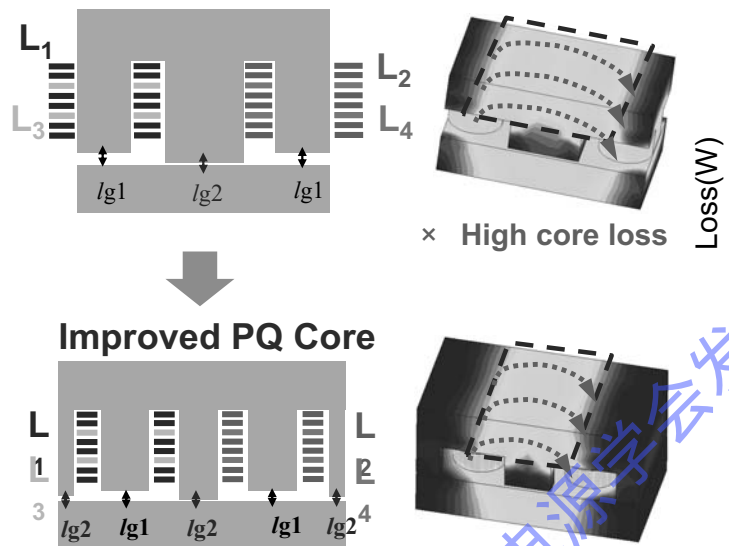
L1 & L2 are positively coupled

Design is different from 1KW PFC

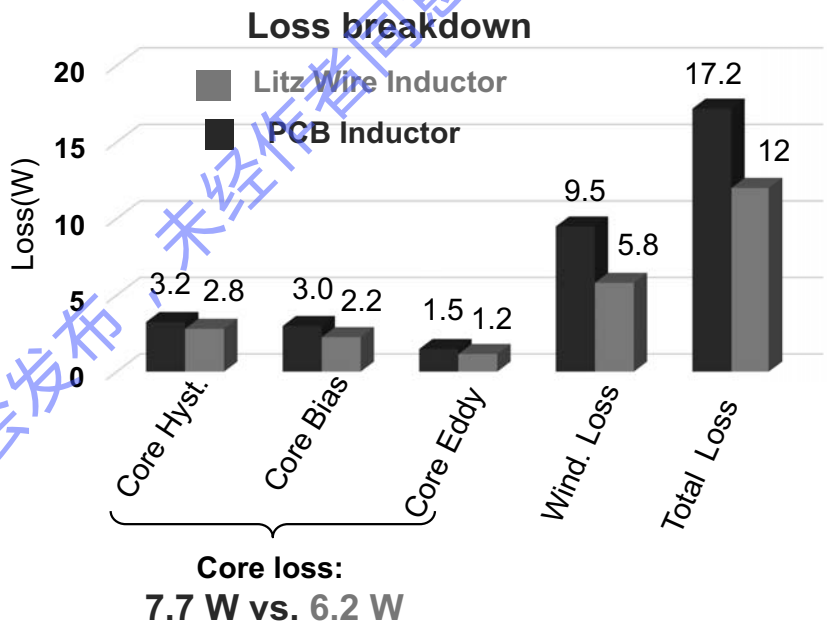


Positive coupling reduces f_{sw} range

3kW PCB Inductor vs. Litz Wire Inductor

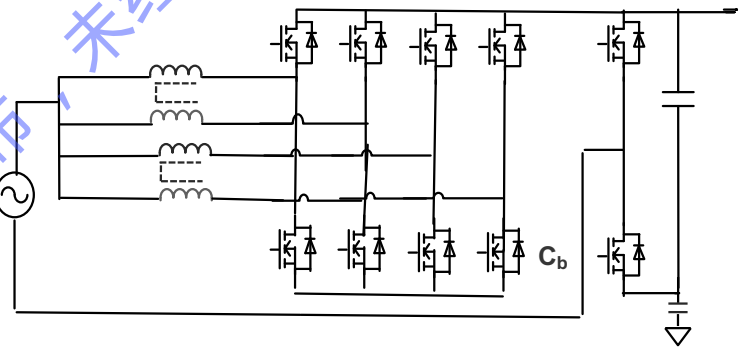
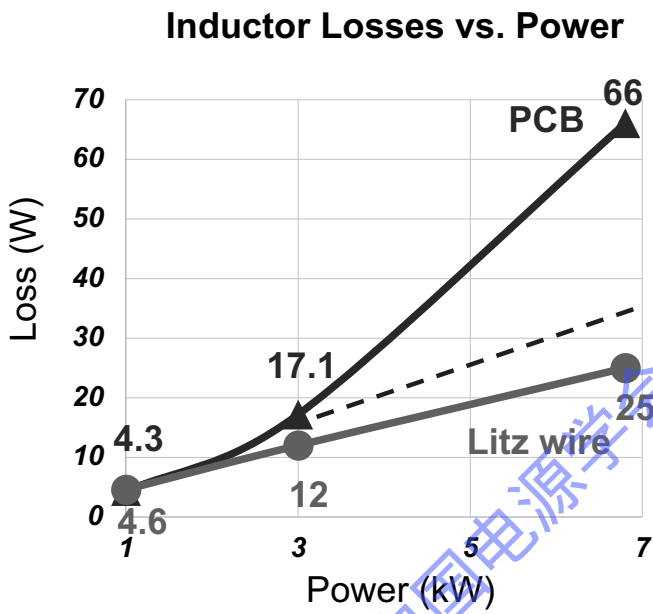


Core loss is reduced by 15%



Limitation: 3KW for PCB Based inductors

Limitation of PCB based Inductors



Maximum power level at 1 KW per phase

Summary

- ❖ PCB Based modular transformer building block @ 1KW
- ❖ PCB Based inductor modular building block @ 1KW

GaN/SiC to Replace Silicon

- ❖ Improvement of Efficiency (incremental)
- ❖ Improvement of Power Density (3-5X)
- ❖ Improvement of EMI/EMC is unique (150KHz- 30MHz)
- ❖ Improvement of Manufacturability - Paradigm shift



Acknowledgement

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Dr. Zhengrong Huang
Dr. Zhengyang Liu

References

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- [3] Yuchen Yang, Mingkai Mu, Zhengyang Liu, Fred Lee, Qiang Li, "Common Mode EMI Reduction Technique for Interleaved MHz Critical Mode PFC Converter with Coupled Inductor," 2015 IEEE Energy Conversion Congress & Expo (ECCE 2015), Montreal, Canada, September 20-24, 2015, pp. 233 - 239.
- [4] Yuchen Yang, Zhengyang Liu, Fred C. Lee, Qiang Li, "Analysis and filter design of differential mode EMI noise for GaN-based interleaved MHz critical mode PFC converter", 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014, pp. 4784 - 4789.
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- [7] Chao Fei, Fred C. Lee, Qiang Li, "High-efficiency High-power-density LLC Converter with an Integrated Planar Matrix Transformer for High Output Current Applications", IEEE Transactions on Industrial Electronics, Vol. 64, No. 11, pp. 9072-9082, November 2017.
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